REMARKS

Applicants' representatives thank Examiner Weiss for the courtesies extended to the undersigned attorney during the personal interview conducted on April 9, 2002. Applicants' separate record of the substance of that interview is incorporated into the following discussion.

Claims 1-19 and 62-79 are pending. The title, specification and claims are amended hereby. A marked-up version showing the changes made by the present amendment is attached hereto as "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

The drawings were objected to due to the description of line A-A' on page 20, lines 1 and 2. The specification has been amended to change this designation so that it corresponds to the designation A-A provided in Fig. 2.

The disclosure has been amended to update the status of the application mentioned on page 20 as U. S. Patent No. 5,780,907. Accordingly, the objection set forth in item 3 of the Office Action has been overcome.

A new title of the invention is provided as required by the Examiner.

The specification has also been amended to include an introductory phrase to the claims. Furthermore, claims 66 and 67 have been amended to overcome the objection noted by the Examiner.

Claims 1-19 and 62-79 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner sets forth specific objections in items 9-15 of the Office Action. The amendments made herein are believed to overcome the specific objections raised by the Examiner. Favorable reconsideration of the rejection is earnestly solicited.

Claims 1-13, 16, 17, 62-65 and 68-73 were rejected under 35 U.S.C. §103(a) as being unpatentable over **Hayashide** in view of **Meguro et al.** In addition, claims 14, 15, 18, 19, 66, 67 and 74-79 were rejected under 35 U.S.C. §103(a) as being unpatentable over these references further in view of **Lee et al.** Favorable reconsideration of these rejections is earnestly solicited.

The Examiner summarizes the teachings **Hayashide** which are considered relevant in the paragraph bridging pages 4 and 5 of the Office Action.

The drawings of **Hayashide** are somewhat difficult to view, particularly in regard to the structure of layers 3-5 and 7. Although it is described that layer 5 is silicon oxide, there does not appear to be a description of layer 7, even though the Examiner characterizes this layer as second insulating films 7 formed on the side walls of the lamination and made of silicon dioxide. Since the drawings of **Hayashide** are difficult to view, applicants extracted Fig. 1 from the counterpart Japanese specification as attached hereto. The attached drawing is slightly better than the U. S. drawing but is still difficult to view. Applicants also drew the related part by handwriting as attached on the basis of their visual observation.

With regard to the basic structure, **Hayashide** is different from the present invention. Namely, **Hayashide** does not disclose the self aligned contact (SAC). On the other hand, the present invention is directed to the insulation structure for the wiring which is suitable for the SAC.

Hayashide simply stacks the silicon oxide film 8, the silicon nitride film 9, BPSG 10 and the silicon oxide film 12 over the gate electrode 4. Then, the contact holes are formed. If the SAC is adopted by **Hayashide**, the sidewall spacers of the silicon oxide and the silicon nitride should be formed at both sides of the wiring by anisotropic etching. However, the silicon oxide film 8 and

the silicon nitride film 9 are laterally extending.

The Examiner pointed out a layer 7 as the sidewall. Although applicants reviewed the U. S. and counterpart Japanese specifications, there is no description relating to the layer 7. Even if the layer 7 is assumed as the claimed second insulating film, the silicon nitride 9 does not cover the layer 7 as required by the claimed pair of fourth insulating films. Therefore, the silicon oxide film 8 is exposed in the contact hole.

In any event, contrary to the Examiner's assertion, **Hayashide** does not appear to disclose a pair of fourth insulating films formed on the pair of side walls of the lamination through said third (in the amended claims) insulating films, to be contiguous to said second (amended claims) insulating film, the second (amended claims) and the fourth insulating films collectively covering the first conductive film. The Examiner considers the film 10 of **Hayashide** as meeting this feature. However, contiguous is defined by the Webster's New Collegiate Dictionary as "being in actual contact ." As such, **Hayashide** fails to teach these features.

The Examiner acknowledges the deficiency of **Hayashide** in the last paragraph on page 5 of the Office Action. More specifically, the Examiner acknowledges that **Hayashide** does not show the second (third in the amended claims) insulating film having a thickness smaller than the first insulating film. It is the Examiner's position that it would have been obvious to form a first insulating film under the bottom of a second or fourth insulating film and defining an aperture based on the teachings of **Meguro et al.** "to improve the strength of the electrodes with respect to external forces." Although the Examiner provides this reason for apparently providing motivation, it does not appear that the teachings of **Meguro et al.** would have motivated one of ordinary skill in the art to have modified **Hayashide** as asserted by the Examiner.

The Examiner relies upon the disclosure at column 2, lines 53-57 of **Meguro et al.** for the alleged motivation to make the modifications "to improve the strength of the electrodes." However, this disclosure does not appear to suggest that the particular modification urged by the Examiner would result in the improvement of the strength of the electrodes with respect to external forces.

The problem which **Meguro et al.** seeks to solve in order to improve the strength of the electrodes with respect to external forces is discussed at column 2, lines 20-52.

Meguro et al. does not disclose a self-aligned contact structure. As such, there would have been no motivation to have combined the references as asserted by the Examiner.

Even if the references could have been combined, the combination fails to teach or suggest the self-aligned contact.

For at least the foregoing reasons, the claimed presently claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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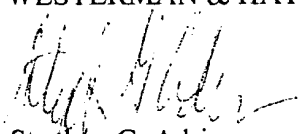

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Attachments: Version with Markings to Show Changes Made
Information Disclosure Statement
Figure from counterpart Japanese specification and handwritten Figure

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VERSION WITH MARKINGS TO SHOW CHANGES MADE (S.N. 09/920,927)

IN THE SPECIFICATION:

Please amend the specification as follows:

Paragraph beginning at page 19, line 22 has been amended as follows:

Next, with reference to Figs. 3A to 13, a method of forming contact windows of DRAM by self align contact (SAC) techniques will be specifically described. Figs. 3A to 13 are schematic cross sectional views showing a memory cell area taken along line [A-A'] A-A of Fig. 2 and a typical wiring structure of a peripheral circuit area. It may be noted that line [A-A'] A-A crosses both the word line 12 and the bit line 13.

Paragraph beginning at page 20, line 13 has been amended as follows:

The p-channel MOS transistor area may be an n-type well formed in a p-type silicon substrate, and the n-channel MOS transistor area may be a p-type well formed in the p-type silicon substrate or a p-type well (triple-well structure) formed in an n-type well in the p-type silicon substrate. These structures may be selected as desired according to the design characteristics. For example, reference may be made to US patent application, Serial Number 08/507,978, filed on July 27, 1995, now U. S. Patent No. 5,780,907, claiming priority of September 22, 1994, which is incorporated herein by reference.

Paragraph beginning at page 61, line 1 has been amended as follows:

[CLAIMS:] We Claim:

IN THE CLAIMS:

The claims have been amended as follows:

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having an uppermost insulating film;

lamination of a first conductive film of metal or metal silicide, a first insulating film, and a ~~third~~ second insulating film made of silicon nitride laminated in this order from a lower side, the lamination being formed on or above the uppermost insulating film, and having a same pattern with a pair of side walls;

a pair of ~~second~~ third insulating films formed on the pair of side walls of the lamination covering at least the first conductive film, the ~~second~~ third insulating film being made of a same material as the first insulating film, and having a thickness smaller than that of the first insulating film;

a pair of fourth insulating films formed on the pair of side walls of the lamination through said ~~second~~ third insulating films, to be contiguous to said ~~third~~ second insulating film, the ~~third~~ second and the fourth insulating films collectively covering the first conductive film;

an interlevel insulating layer formed on or above said semiconductor substrate, covering said ~~third~~ second and fourth insulating films;

an aperture formed through said interlevel insulating layer, at least partially exposing one of said fourth insulating films; and

a second conductive film filling the aperture.

2. (Amended) A semiconductor device according to claim 1, wherein said first insulating film ~~covers~~ and said pair of third insulating films cover the side wall and upper surface of said first conductive ~~pattern~~ film.

3. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having an uppermost insulating film;

lamination of a first conductive film made of metal or metal silicide, a first insulating film, and a ~~third~~ second insulating film made of silicon nitride laminated in this order from a lower side, the lamination being formed on or above the uppermost insulating film, and having a same pattern with a pair of side walls;

a pair of ~~second~~ third insulating films formed on the pair of side walls of the lamination covering at least the first conductive film, the ~~second~~ third insulating film having a thickness smaller than that of the first insulating film, the first and ~~second~~ third insulating films being made of different materials except silicon nitride;

a pair of fourth insulating films formed on the pair of side walls of the lamination through said ~~second~~ third insulating films, to be contiguous to said ~~third~~ second insulating film, the ~~third~~ second and the fourth insulating films collectively covering the first conductive film;

an interlevel insulating layer formed on or above said semiconductor substrate, covering said ~~third~~ second and fourth insulating films;

an aperture formed through said interlevel insulating layer, at least partially exposing one of said fourth insulating films; and

a second conductive film filling the aperture.

4. (Amended) A semiconductor device according to claim 1, wherein said ~~first~~ third insulating film extends under a bottom end of said ~~second~~ fourth insulating film positioned on the side wall of said first conductive ~~pattern~~ film.

5. (Amended) A semiconductor device according to claim 1, wherein said first conductive ~~pattern~~ film is a gate electrode of a MIS transistor.

6. (Amended) A semiconductor device according to claim 1, wherein said ~~first~~ third insulating film is made of a silicon oxide film.

8. (Amended) A semiconductor device according to claim 1, ~~further comprising: a third insulating film having~~ wherein said interlevel insulating film has etching characteristics different from a silicon nitride film and is formed on said second insulating film made of a silicon nitride ~~film; and~~

~~a contact area formed in said third insulating film, having a bottom portion at least partially defined by said second insulating film.~~

9. (Amended) A semiconductor device according to claim 8, wherein the surface of said ~~third insulating film~~ interlevel insulating layer is generally parallel to said semiconductor substrate.

11. (Amended) A semiconductor device according to claim ~~10~~ 8, further comprising:

a ~~fourth~~ fifth insulating film formed on the ~~third insulating film~~ interlevel insulation layer and defining a contact area on said second conductive ~~plug~~ film.

12. (Amended) A semiconductor device according to claim 11, further comprising:

an upper conductive pattern formed on said ~~fourth~~ fifth insulating film and on said second conductive ~~plug~~ film;

a ~~fifth~~ sixth insulating film made of an insulating material other than silicon nitride, and formed to cover at least a side wall of said upper conductive pattern; and

a ~~sixth~~ seventh insulating film made of silicon nitride and formed to continuously cover said upper conductive pattern and said ~~fifth~~ sixth insulating film.

13. (Amended) A semiconductor device according to claim 12, further comprising:

another contact area formed in said ~~third insulating film~~ interlevel insulating layer on an opposite side of said first conductive ~~pattern~~ film to said contact area, having a bottom portion at least partially defined by said ~~second~~ fourth insulating film; and

another conductive ~~plug~~ film filling said another contact area;

wherein said ~~fourth~~ fifth insulating film further defines another contact area on said another conductive ~~plug~~ film.

14. (Amended) A semiconductor device according to claim 13, further comprising a storage capacitor formed on said another conductive ~~plug~~ film.

15. (Amended) A semiconductor device according to claim 14, wherein said storage capacitor is formed to at least partially cover said ~~sixth~~ seventh insulating film.

16. (Amended) A semiconductor device according to claim 12, further comprising:

~~seventh~~ an eighth insulating film made of silicon nitride formed between said ~~third~~ interlevel insulating film and ~~fourth~~ fifth insulating ~~films~~ film, and cooperatively defining said contact area with said ~~third insulating film~~ interlevel insulating layer.

17. (Amended) A semiconductor device according to claim ~~12~~ 14 , further comprising:

a field insulating film formed on a surface of said semiconductor substrate, and having a surface at a higher level than said insulating surface of said substrate;

wiring patterns formed on said field insulating film and on said ~~fourth~~ fifth insulating film; and

silicon nitride layers covering said wiring patterns.

18. (Amended) A semiconductor device according to claim 17, further comprising:

an interlayer insulating layer covering said ~~fourth~~ fifth insulating layer, said storage capacitor, and said silicon nitride layer covering the wiring pattern on said ~~fourth~~ fifth insulating film;

connection holes formed through said interlayer insulating layer and reaching said wiring patterns; and

upper wiring patterns ~~filling said connection holes~~.

19. (Amended) A semiconductor device according to claim 18, wherein said storage capacitor includes a storage electrode connected to said another conductive ~~plug~~ film, a dielectric film formed on said storage electrode and on said ~~fourth~~ fifth insulating film, and an opposing electrode formed on said dielectric film and having an extension on said ~~fourth~~ fifth insulating film, one of said connection holes penetrates through said opposing electrode at said extension, and one of said upper wiring patterns makes electrical contact with said opposing electrode at its side wall.

62. (Amended) A semiconductor device according to claim 3, wherein said ~~second~~ third insulating film extends under a bottom end of said fourth insulating film positioned on the side wall of said lamination.

63. (Amended) A semiconductor device according to claim 3, wherein said first conductive ~~pattern~~ film is a gate electrode of a MIS transistor.

64. (Amended) A semiconductor device according to claim 3, wherein said ~~second~~ third insulating film is made of a silicon oxide film.

65. (Amended) A semiconductor device according to claim 3, wherein said interlevel insulating layer has etching characteristics different from a silicon nitride film and is formed on said ~~third~~ second insulating film made of a silicon nitride.

66. (Amended) A semiconductor device according to claim 1, wherein said first conductive ~~pattern~~ film forms a bit line of a dynamic random access memory.

67. (Amended) A semiconductor device according to claim 3, wherein said first conductive ~~pattern~~ film forms a bit line of a dynamic random access memory.

68. (Not Amended) A semiconductor device according to claim 3, wherein the first insulating film is made of silicon oxy-nitride.

69 (Not Amended) A semiconductor device according to claim 3, wherein the surface of said interlevel insulating layer is generally parallel to said semiconductor substrate.

71. (Amended) A semiconductor device according to claim ~~70~~ 65, further comprising:

a fifth insulating film formed on the interlevel insulation layer and defining a contact area on said second conductive ~~plug~~ film.

72. (Amended) A semiconductor device according to claim 71, further comprising:

an upper conductive pattern formed on said fifth insulating film and on said second conductive ~~plug~~ film;

a sixth insulating film made of an insulating material other than silicon nitride, and formed to cover at least a side wall of said upper conductive pattern; and

a seventh insulating film made of silicon nitride and formed to continuously cover said upper conductive pattern and said sixth insulating film

73. (Amended) A semiconductor device according to claim 72, further comprising:

another contact area formed in said interlevel insulating layer on an opposite side of said first conductive ~~pattern~~ film to said contact area, having a bottom portion at least partially defined by said fourth insulating film; and

another conductive ~~plug~~ film filling said another contact area;

wherein said fifth insulating film further defines another contact area on said another conductive ~~plug~~ film.

74. (Amended) A semiconductor device according to claim 73, further comprising a storage capacitor formed on said another conductive ~~plug~~ film.

75. (Not Amended) A semiconductor device according to claim 74, wherein said storage capacitor is formed to at least partially cover said seventh insulating film.

76. (Not Amended) A semiconductor according to claim 75, further comprising:

an eighth insulating film made of silicon nitride, formed between said fourth and fifth insulating films, and cooperatively defining said contact area with said fourth insulating film.

77. (Not Amended) A semiconductor device according to claim 76, further comprising:

a field insulating film formed on a surface of said semiconductor substrate, and having a surface at a higher level than said insulating surface of said substrate;

wiring patterns formed on said field insulating film and on said fifth insulating film; and

silicon nitride layers covering said wiring patterns.

78. (Not Amended) A semiconductor device according to claim 77, further comprising:

an interlayer insulating layer covering said fifth insulating layer, said storage capacitor, and said silicon nitride layer covering the wiring pattern on said fifth insulating film;

connection holes formed through said interlayer insulating layer and reaching said wiring patterns; and

upper wiring patterns.

79. (Amended) A semiconductor device according to claim 78, wherein said storage capacitor includes a storage electrode connected to said another conductive ~~plug~~ film, a dielectric film formed on said storage electrode and on said fifth insulating film, and an opposing electrode formed on said dielectric film having an extension on said fifth insulating film one of said connection holes penetrates through said opposing electrode at said extension, and one of said upper wiring patterns makes electrical contact with said opposing electrode at its side wall.